WHAT IS CLAIMED:

1. A data processing system comprising:

a data transferring apparatus having data input and data output; a plurality of data transferring sections operable in parallel for transferring data, and a circuit for synchronising said parallel data transferring sections; and

a programmable frequency clock generator for generating a clock signal, wherein said programmed frequency includes a full-frequency and a low-frequency, the low frequency being a quotient of the full frequency and the number of said data transferring sections;

wherein said data transferring sections operate at said low frequency; while said input and output data are provided at said full frequency.

2. The data processing system according to claim 1, wherein said data transferring sections are data transmitters.

3. The data processing system according to claim 1, further comprising a multiplexer for receiving data from said data transferring sections at said low frequency and providing output data at said full frequency.

4. The data processing system according to claim 1, when used as a test system, wherein said data is transferred at said full frequency for accessing a memory device under test.

5. The data processing system according to claim 1, wherein said data transferring sections are data receivers.

6. The data processing system according to claim 1, wherein the data transferring apparatus comprises a plurality of data transmitting sections and a plurality of data receiving sections, wherein said data transmitting sections and said data receiving sections are operable at said low frequency; while said output and input data is transferred at said full frequency.

7. The data processing system as claimed in claim 1, wherein said low frequency is equal to a half of said full frequency.

8. The data processing system as claimed in claim 1, wherein said low frequency is equal to one forth of the full frequency.

9. The data processing system as claimed in claim 1, further comprising a resynchronisation circuit for resynchronising data received at low frequency to a system clock signal of full frequency.

10. A method of data processing comprising the steps of:

providing input data and output data;

transferring data through a plurality of parallel data transferring channels, wherein the data transfer additionally comprises synchronising said parallel data transferring channels;

generating clock signals of programmable frequency, wherein said programmed frequency includes full-frequency and low-frequency, the low frequency being a quotient of the full frequency and the number of said data transferring channels,

wherein said operations of data transfer are performed at said low frequency, while said input and output data are provided at said full frequency.

11. The method of data processing according to claim 10, wherein the data transferring sections are data transmitters, the method further comprising multiplexing data received from said data transmitters at said low frequency and providing multiplexed output data at said full frequency.

12. The method of data processing according to claim 10, wherein the data at said full frequency are provided for accessing memory device under test.

13. The method of data processing according to claim 10, wherein the data transferring sections are data receivers comprising a plurality of registers for latching data from a memory device under test and the latched fault data are supplied to a plurality of fault logic devices.

14. The method of data processing according to claim 10, comprising the steps of transmitting data, latching transmitted data and supplying latched data to a plurality of receiving logic devices; wherein said operations of data transmission, latching data and receiving data are performed at said low frequency; while said input and output data are provided at said full frequency.

15. The method of data processing according to claim 1, wherein said low frequency is equal to a half of said full frequency, for SDRAM memories.

16. The method of data processing according to claim 1, wherein said low frequency is equal to one forth of the full frequency, for DDR memories.

17. The method of data processing according to claim 1, further comprising a step of resynchronisation of data received at low frequency to a system clock signal of full frequency.

18. A test system comprising:

an algorithmic pattern generator having a plurality of test data generating sections operable in parallel for generating test data for accessing a memory device under test, wherein the pattern generator additionally comprises a circuit for synchronising said parallel data generating sections;

a programmable frequency clock generator for generating a clock signal, wherein said programmed frequency includes a full-frequency and a low-frequency, the low frequency being a quotient of the full frequency and a number of said test data generating sections;

a multiplexer that receives said test data from said data generating sections at said low frequency and provides multiplexed data for accessing DUT at said full frequency;

a plurality of registers for latching data from the DUT and supplying latched fault data to a plurality of fault logic devices;

wherein said test data generating sections, said registers and said fault logic devices operate at said low frequency; while said device under test is accessed at said full frequency.

19. The test system as claimed in claim 18, wherein said low frequency is equal to a half of said full frequency, for example, for SDRAM memories.

20. The test system as claimed in claim 18, wherein said low frequency is equal to one forth of the full frequency, for DDR memories.